1. (currently amended) A method, comprising:

assigning a plurality of nodes within a storage circuit to a predetermined state, while a clock signal is at a first level;

evaluating a plurality of signals coupled to the storage circuit, when the clock signal is at a second level, wherein evaluating the plurality of signals enables a first node to change from its predetermined state ~~and enables a second node to be more susceptible to perturbations~~; and

actively maintaining ~~the~~ a second node continuously in its predetermined state, ~~for a predetermined period of time, wherein maintaining the predetermined state reduces the storage circuit's susceptibility to soft errors~~ from a time before the clock signal changes from the first level to the second level, until a time after the first node changes from its predetermined state.

2 - 9 (canceled)

10. (currently amended) A storage circuit, comprising:

a plurality of nodes including a first node and a second node, wherein the second node is coupled to the first node;

~~a plurality of signals coupled to~~ the storage circuit receiving a plurality of signals, wherein the signals enable a first node to change from a predetermined state to a second state; and

a circuit element coupled to the second node, wherein the circuit element actively maintains the second node at its predetermined state ~~for a predetermined period of time~~ continuously from a time before the first node starts changing from its predetermined state until a time after the first node changes from its predetermined state.

11 - 15 (canceled)

16. (currently amended) A computer system, comprising:

a processor;

a system memory coupled to said processor, wherein the memory further comprises:

a plurality of nodes;

a timing signal; and

~~at least one~~ a plurality of control signals;

wherein the timing signal and the control signals cause a first node within the plurality to change from an initialized state to a finalized state while a second node within the plurality is actively maintained in an initial state, continuously from a time before the timing signal causes the first node to start changing to its finalized state until a time after the first node changes to its finalized state~~; and~~

~~wherein maintaining the second node while the first node is changing reduces the storage circuit's susceptibility to soft errors~~.

17-22 (canceled)

23. (new) The method of claim 1, wherein the second node is actively maintained in its predetermined state by one of the plurality of signals and the state of the second node.

24. (new) The method of claim 1, further comprising:

delaying, for a predetermined time after the clock signal changes to its second level, a signal that causes circuitry to actively maintain a node in a second state other than the predetermined state.

25. (new) The storage circuit of claim 10, wherein the circuit element coupled to the second node actively maintains the second node at its predetermined state in response to one of the plurality of signals and the state of the second node.

26. (new) The storage circuit of claim 10, further comprising:

a circuit element, coupled to the second node, that can actively maintain the second node in a second state, in response to a delayed signal from the second node.

27. (new) The storage circuit of claim 26, wherein at least one transistor in the circuit element that maintains the second note at its predetermined state is larger than any transistor in the circuit element that can actively maintain the second node in a second state.

28. (new) The computer system of claim 16 wherein the second node is actively maintained in its initial state in response to one of the control signals and the state of the second node.

29. (new) A method comprising:

driving a plurality of nodes in a storage circuit to a precharge state when a clock signal is at a first level;

driving a first node in the plurality of nodes to a second state, in response to a first input signal, when the clock signal changes from the first level to a second level; and

driving a second node in the plurality of nodes to the precharge state by a second input signal and by a signal corresponding to the state of the second node.